

TRANSMITTAL

Electronic Version v1.1

Stylesheet Version v1.1.0

Title of Invention	SELF-ALIGNED DRAIN/CHANNEL JUNCTION IN VERTICAL PASS TRANSISTOR DRAM CELL DESIGN FOR DEVICE SCALING	
Application Number :		
Date :		
First Named Applicant:	Geng Wang	
Confirmation Number:		
Attorney Docket Number:	FIS920030209US1	
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		Sign. Capacity Agent

Documents being submitted:	Files
us-fee-sheet	FIS920030209US1-usfees.xml us-fee-sheet.xsl us-fee-sheet.dtd
us-ids	FIS920030209US1-usidst.xml us-ids.dtd us-ids.xsl
us-request	FIS920030209US1-usrequ.xml us-request.dtd us-request.xsl
us-declaration	fis920030209us1declaration1.tif
us-declaration	fis920030209us1declaration2.tif
us-declaration	fis920030209us1declaration3.tif
application-body	FIS920030209US1-trans.xml us-application-body.xsl application-body.dtd wipo.ent mathml2.dtd mathml2-qname-1.mod isoamsa.ent isoamsb.ent isoamsc.ent isoamsn.ent isoamso.ent isoamsr.ent isogr3.ent isomfrk.ent isomopf.ent isomscr.ent isotech.ent isobox.ent isocyr1.ent isocyr2.ent isodia.ent isolat1.ent isolat2.ent isonum.ent isopub.ent mmlextra.ent mmlalias.ent soextblx.dtd FIS920030209US1Drawing1.tif FIS920030209US1Drawing2.tif FIS920030209US1Drawing3.tif FIS920030209US1Drawing4.tif FIS920030209US1Drawing5.tif FIS920030209US1Drawing6.tif FIS920030209US1Drawing7.tif FIS920030209US1Drawing8.tif FIS920030209US1Drawing9.tif

Comments

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